

Main Draw				
1	TSA081544	KZN	Aiden MARAIS	
2			A1 BYE	Aiden MARAIS
3	TSAJJ2063		 Andries Ignatius Wilhelmus FER	Liam VENTER 6-0, 6-1
4	TSA071715	GN	Liam VENTER	Liam VENTER 6-4, 6-1
5	TSA071739	GC	 Daniel ROEBL	Daniel ROEBL 2-6, 6-2, 11-9
6			A3 BYE	Daniel ROEBL
7	TSA081170		Samuel OSSIP	Daniel ROEBL 6-4, 6-2
8			A4 BYE	Samuel OSSIP
9	TSA071709	GN	Waldo DU PLESSIS	Waldo DU PLESSIS 6-4, 6-1
10			A5 BYE	Waldo DU PLESSIS
11			BYE	Waldo DU PLESSIS 6-3, 6-2
12	TSA081542	GC	 Vihar NAIDU	Vihar NAIDU
13	TSAJJ2053		 Francois Marcus FERREIRA	Waldo DU PLESSIS 5-7, 6-4, 10-5
14	TSA071735	GN	 Christiaan SIME	Francois Marcus FERREIRA 6-3, 2-6, 10-5
15			BYE	Thyan BOTHA 6-2, 6-4
16	TSA071740	LIM	 Thyan BOTHA	Thyan BOTHA

Liam VENTER	
	Thyan BOTHA
Thyan BOTHA	6-1, 6-2

Aiden MARAIS	Samuel OSSIP	
Samuel OSSIP	6-2, 6-0	
Vihar NAIDU		Francois Marcus FERREIRA
		6-2, 2-6, 10-4
Francois Marcus FERREIRA	Francois Marcus FERREIRA	
	7-5, 6-2	

Aiden MARAIS	
Vihar NAIDU	6-4, 6-0



BYE			
E1	Andries Ignatius Wilhelmus FEF		
Andries Ignatius Wilhelmus FEF			
	E5	Andries Ignatius Wilhelmus FER	
BYE			
E2	BYE		
BYE			
			Andries Ignatius Wilhelmus FER
			6-7, 7-5, 10-5
BYE			
E3	BYE		
BYE			
	E6	Christiaan SIME	
Christiaan SIME			
E4	Christiaan SIME		
BYE			

BYE

F1
BYE

The diagram illustrates a 3-bit bus system with three masters (G1, G2, G3) and one slave. The bus width is 3 bits. The diagram shows the timing of data and control signals. The 'BYE' signal is active low, indicating the end of a transfer. The data signals are shown as 3-bit buses. The diagram shows a sequence of data transfers where G1 and G2 transfer data to the slave, and then G3 transfers data to the slave. The 'BYE' signals indicate the end of each transfer.

BYE	
H1	
BYE	

